The Level 1 Muon Trigger System for Run II of DØ

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for the DØ Collaboration

- Level 1 Architecture
- Design Features
- Simulation Results
Muon Detector Upgrade

Forward Trigger Scint (Pixels)

Shielding

Forward Tracker (MDTs)

Bottom B/C Scint

Central Trigger Scint ($A-\phi$)

PDTs

Fiber Tracker
7 MHz, 132 ns crossing times

Accommodate:
$L=2 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$ &
Bunch Crossings 132 ns.
Deadtime: $<10\%$
Specifications

• Deliver a trigger decision to the Trigger Framework 3.3 μs after each bunch crossing
• Buffer data pending L1 and L2 decisions
• Incur no deadtime
• Contain field programmable logic
• Goal is to provide:
  ❖ Unprescaled high $P_T$ single muon trigger and
  ❖ Unprescaled low $P_T$ dimuon trigger for as large a rapidity range as possible
L1 Muon Trigger

Gbit/s Serial Link
Inputs from Muon
Front End, Central
Fiber Tracker

Programmable
Logic Downloading
and User
Communication via
1553 system

Octant Trigger
Card
(x8)

Regional
Trigger
Card

Global
Trigger
Card

Level 2
Muon
Trigger

Muon
Readout
Crate

To Trigger
Framework
(TF)

To Global
L2 Trigger

To L3
Trigger

Timing and
TF Messages

Trigger Data

Regional
Trigger
Card
Design Features

• Each trigger card must accept a large amount of information - ~1600 bits per 132ns bunch crossing

• Use Gbit/s serial links
  ◆ Transmit data over up to 150’ of copper coaxial cable (LMR-200)
  ◆ Use amplifier / equalizer circuit on receiver to recover signal
  ◆ Bit error rate < $10^{-14}$ at 150’
Gbit/s Serial Links

Eye Patterns

After 150' of LMR-200, no amp./eq.

After 150' of LMR-200, with amp./eq.
Triggers

- Form triggers based on wire and scintillator hits and L1 Central Fiber Tracks
  - Two trigger cards / octant
    - “scint” - match L1CFT with scintillator hits for various $P_T$ thresholds
    - “wire” - scintillator confirmed wire coincidences
  - Both scint and wire triggers are formed with various qualities based on number of coincident layers hit

- Use Field Programmable Gate Arrays (FPGA’s) to form triggers
  - Implement logic on 4-7 Altera ACEX or FLEX 10KA devices
  - Process input data on 18.8 ns clock
  - Logic takes ~600 ns to complete
Muon Trigger Card

Flavor Board w/ FPGA's

Serial links

Coaxial inputs

Custom J2 backplane
# Simulation

C, +, 1–15 GeV/c, LL LI MU Trig. and Accep. PT

| # Muons | Pt (GeV/c) | $|\eta|\ $ | Rate (kHz) |
|---------|-----------|---------|-----------|
| 1       | >11       | <1.0    | 0.2       |
| 1       | >11       | <1.5    | 0.2       |
| 2       | >2        | <1.0    | 2.0       |
| 2       | >2        | <1.5    | 4.8       |

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Conclusions

- The L1Muon Trigger system uses hits from all muon detectors and tracks from the L1 Central Fiber Tracker Trigger
  - Use Gbit/s serial links to receive input data over copper coax
  - Form triggers with various $P_T$ thresholds and qualities
  - Logic implemented in Field Programmable Gate Arrays
- Preliminary simulation rates and efficiencies look good
- Commissioning with pre-production boards underway