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& INFN
BARI
on behalf of the
CMS Silicon Tracker Collaboration
December 1999: baseline solution ⇒ all-silicon solution

Baseline solution

- Pixel vertex detector, inner silicon tracker, outer MSGC tracker

All-silicon solution

- Pixel vertex detector, inner + outer silicon tracker

Motivations

- 6” production lines available
- Progress of automatic procedure in module assembling & testing
- Excellent performances of the silicon sensors readout chip (APV25)
Outline

- silicon tracker layout
- silicon sensors specifications
- bulk resistivity & depletion voltage
- strip capacitance & expected Signal to Noise ratio
- crystal lattice orientation & interstrip capacitance
- breakdown voltage
- conclusions
All-Silicon Layout

sensor multiplicity:

IB: 2808
IF: 3328

320 μm

OB: 11856
OF: 7776

500 μm

~ 200 m² active silicon

~ 20000 modules
charged hadrons fluences

expected fluences for $L=5 \times 10^5$ pb$^{-1}$ (10 years)

innermost layer will receive a fluence of $1.6 \times 10^{14}$ n(1 MeV)/cm$^2$

damage

neutrons fluences

bulk

formation of trapped charge

surface

type inversion

rising depletion voltage

interstrip capacitance
Sensors Specifications

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<th></th>
<th>inner tracker</th>
<th>outer tracker</th>
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<tbody>
<tr>
<td></td>
<td>only single-sided</td>
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<tr>
<td></td>
<td>double-sided modules: 2 single-sided modules back-to-back</td>
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<td></td>
<td>$p^+$ on n-type</td>
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<tr>
<td></td>
<td>$\rho \sim 2 , \text{k,cm (LR)}$</td>
<td>$\rho \sim 4 , \text{k,cm (HR)}$</td>
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<tr>
<td></td>
<td>$&lt;100&gt;$ crystal lattice orientation</td>
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<td></td>
<td>AC coupling</td>
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<tr>
<td></td>
<td>polysilicon resistors ($\sim 1.5 , \text{M,\Omega}$)</td>
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<tr>
<td></td>
<td>strip width/pitch $\sim 0.25$</td>
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<td></td>
<td>metal overhang ($\sim 4 \div 8 , \mu\text{m}$)</td>
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<td></td>
<td>depletion voltage $&lt; 250 , \text{V}$</td>
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<td></td>
<td>breakdown voltage $\geq 500 , \text{V}$</td>
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</table>
Bulk Resistivity

role: depletion voltage

$N_{\text{eff}}$ change with fluence

$\Rightarrow$ depletion voltage change with fluence

LR bulks show $V_{\text{dep}} < V_{\text{breakdown}}$ also after 10 years at LHC

lines are drawn to guide the eye
Inner Sensors

low resistivity (~ 2 kΩ cm) sensors for the inner tracker due to higher radiation levels:

\[ R \sim 20 \text{ cm} \quad \Phi \sim 1.6 \times 10^{14} \text{ n}(1 \text{ MeV})/\text{cm}^2 \]

⇒ 1 inner tracker module: 1x6” sensor or 2x4” sensors
⇒ ~ 10 cm strip length

\[ I \sim 1.0 \mu\text{A}/\text{strip} \ (T = -10 \, ^{\circ}\text{C}) \quad \Leftrightarrow \ 350 \, \text{e}^- \]

main contribution to the noise is due to the total strip capacitance
**Outer Sensors**

high resistivity (\( \sim 4 \, \text{k}\Omega \, \text{cm} \)) sensors for the outer tracker due to lower radiation levels:

\[ R > 100 \, \text{cm} \quad \Phi < 4 \times 10^{13} \, \text{n/cm}^2 \]

\( \Rightarrow \) depletion voltage does not increase as for the inner tracker sensors

\[ V_{\text{dep before irradiation}} \sim 120 \, \text{V} \quad V_{\text{dep after irradiation}} \sim 180 \, \text{V} \quad (400 \div 500 \, \mu\text{m}) \]

\( \Rightarrow \) 1 outer tracker module: 2x6” sensors

\( \Rightarrow \) \( \sim 16 \) cm strip length

after \( 5 \times 10^{13} \, \text{n/cm}^2 \) \( I \sim 1.5 \, \mu\text{A/strip} \) \((T = -10^\circ \text{C})\) \( \Leftrightarrow 500 \, \text{e}^- \)

main contribution to the noise is the total strip capacitance as for the inner tracker sensors
Sensors Capacitance

Experimental results show that:

\( C_{\text{tot}} \) is function only of the width/pitch ratio

- Interplay between \( C_{\text{int}} \) and \( C_{\text{back}} \)
- \( C_{\text{tot}} \) pitch independent
- Independent also of thickness at least for pitch smaller than thickness

Parametrization for real strip (not perfect planar diode)
Total Capacitance

Measurement conditions:
- $V_{bias} \sim 500$ V
- 1 MHz

Total capacitance does not depend on fluence for $\langle 100 \rangle$ devices.

6" wafer production lines are of the same high quality as the 4" ones.
Signal to Noise

\[ \text{w/p } \sim 0.25 \]

\[ C_{\text{tot}} = 1.26 \text{ pF/cm} \times \text{(strip length)} \]

\[ \begin{aligned}
1360 \text{ e}^- & \quad \text{inner} \\
1660 \text{ e}^- & \quad \text{outer}
\end{aligned} \]

\[ \begin{aligned}
16 \text{ pF} & \quad \text{inner} \\
20 \text{ pF} & \quad \text{outer}
\end{aligned} \]

APV25: \(400 + 60 \times C_{\text{tot}}\) (e-)

\[ \Rightarrow \quad \text{ENC}_{\text{tot}} \sim 1600 \text{ e}^- \quad \text{inner} \]

\[ \sim 1870 \text{ e}^- \quad \text{outer} \quad \Rightarrow \text{thicker sensors} \Rightarrow \text{more signal (30\%)} \]

\[ \begin{aligned}
\text{S/N (expected)} & \sim 13 \quad \text{inner} \\
& \sim 15 \quad \text{outer}
\end{aligned} \]

metal strip resistance: 500 e-

\(I_{\text{leak}}\): 350 e-

optical link: 600 e-
Crystal Lattice Orientation

role: interface SiO$_2$-Si

dangling bonds

⇒ after irradiation trapping levels at interface increase
⇒ higher charge accumulation

$<111>$: $\sim 10^{11}$ charges/cm$^2$

$<100>$: $\sim 10^{10}$ charges/cm$^2$

$C_{\text{int}}^{<100>} < C_{\text{int}}^{<111>}$

(if the quality of the oxide is good)
Interstrip Capacitance

Fluences $\times 10^{14}$ n(1 MeV)/cm$^2$

- $\Phi_0$: 0
- $\Phi_1$: 0.1
- $\Phi_2$: 0.4
- $\Phi_3$: 0.9
- $\Phi_4$: 1.0
- $\Phi_5$: 1.5

- $<100>$ low resistivity
- $<111>$ low resistivity
- $<111>$ high resistivity

$V_{\text{bias}}$ (V)

- $\sim 140$
- $\sim 320$ (90 $V_{\text{dep}}$)
- $\sim 400$ (180 $V_{\text{dep}}$)

$C_{\text{int}} \sim 1.5$ pF

- HR 111
- LR 111
- LR 100
Backplane Capacitance

very small changes before and after irradiation
Breakdown Voltage

High voltage operation is needed, ~ 400 V

For high resistivity outer sensors after type inversion with the increase of effective carriers density

For low resistivity inner sensors the initial depletion voltage will be around 300 V

The data collected in beam tests have shown that the charge collection efficiency can be improved for all sensors well above the nominal depletion voltage

At very high voltages breakdown can happen near the guard-ring and around the strips

First effect is reduced by the use of a multi-guard design

Second effect is reduced by use of metal overhang
**Breakdown Voltage**

*4” devices - 320 μm thick - LR*  
irradiated at $4 \times 10^{14} \text{ p(24 GeV)/cm}^2$

*6” devices - 320 μm thick - LR*  
irradiated at $1.5 \times 10^{14} \text{ p(24 GeV)/cm}^2$

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- **with metal-overhang**  
highest BKD voltage
- **with w/p > 0.2**  
good BKD performances
Breakdown Voltage

6" devices-410 μm thick- HR
irradiated at $1.5 \times 10^{14}$ p(24 GeV)/cm$^2$

$V_{bdwn}$ (V)

240 μm

120 μm

w/p ≥ 0.2 & p ≤ 120 μm
stable operation up to 600 V

BKD > 400 V
Conclusions

CMS silicon tracker will be based on:

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<th>HR sensors ↔ outer layers</th>
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<td>low depletion voltage</td>
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<td>after irradiation</td>
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<th>&lt;100&gt; crystal lattice orientation</th>
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<td>strip capacitance (noise)</td>
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<td>fluence independent</td>
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<td>high voltage stability</td>
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