DDU2004 Status

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**DDU Functions**

- **What does the DDU do?**
  - High-Bandwidth data concentration
    - 15 DMB \(\rightarrow\) DAQ via DCC, capable of continuous 640 MB/sec rate
  - Full error checking and status monitoring
    - CRC check, word count, event number, overflow, link status
  - FMM communication path for EMU DAQ
  - PC data readout via Gigabit Ethernet (local DAQ path)
First 9U DDU Board. Produced and tested in 2002, used for beam tests at CERN in 2003.

- Full error checking implemented
- Interface to VME
- PC readout via Gigabit Ethernet (90 MB/s data transfer)
- DMB calibration pulses, regular and random timing
- S-Link64 tested
  - Need to integrate w/ FMM and TTS

- Worked well in beam tests
- Needs additional functionality for use at LHC
  - New Virtex2 FPGAs can provide more consistent timing
  - More logic at input stage can provide better stability in case of bit errors
Fiber links from 15 DMBs

FPGA

FPGA

FPGA

FIFO

FIFO

CCB/TTC via Backplane

S-Link

Gigabit Ethernet To Local DAQ

FMM/Slow Control

JTAG via VME

DCC/DAQ via Backplane

BUSY

READY

L1 Throttle

Data Errors

Loss of Synch
**DDU2004 Prototype**

- **VME FPGA**: XILINX Virtex2-500
- **DMB Input FPGAs**: 2 XILINX Virtex2Pro-20
- **4 Input FIFOs**: 512 KB each
- **GBE FIFO**: 1024 KB

**Components**:
- **DDU Control FPGA**: XILINX Virtex2Pro-7
- **Gbit Ethernet Output**: To Local DAQ
- **SLINK Mezzanine board connector**
- **FMM output port**
- **15 Optical fiber inputs (just 1 for now)**
DDU2004 Plan

• Old DDU Design
  ✓ 2 Virtex-E FPGAs, 16 FIFOs, 17 ball-grid arrays!
    • NO ball-grid problems out of ~4800 ball-grid solder joints

• Improvements in DDU2004 Prototype
  – Faster FPGAs & FIFOs, better timing
  – 4 FPGAs, 5 FIFOs, 9 ball-grid arrays
    • ~3700 ball-grid solder joints
  – Better data-loss handling
    • Allows recovery from data loss without reset
  – Implement two-way fiber communication
    • DMB-DDU and also DDU-DMB for feedback/control
  – Less expensive than previous design

➢ All FPGAs programmed, hardware and firmware testing continues...