Who are we?

- Paul Nylander -- HW Design & SW Implementation
- Dan Herman -- HW Engineering
- etc. (OSU CMS Group & OSU Electronics Shop)

Status of Summer Test Beam Readout Hardware

The CMS EMU CSC DDU from OSU

...and other three letter words

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CFEBs

(J. Gu)

Anode Trigger

Cathode Trigger

(not to scale)
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“DDU Features”
- 75 MHz X 16-bit PLL Optical Link (HP GLink, HP Optical Transceiver)
- Supplies 75 MHz clock to DAQ-MB via PLL Optical System
- 16-bit X 64 kWord RXFIFO (at 75 MHz) (word = 16-bit)
- AMCC S5933 PCI Interface (32 bits, 33 MHz)
  - Automatic “Alternate Word” Filling (16 to 32 Bits)
  - 32-bit X 8 Word FIFO
  - Allows 66 MWord/s burst for 16 - 20 words (word = 16-bits)
- Low level (word-by-word) error checking built into GLink
- Linux PCI Driver code based on A. Cisterino’s AMCC S5933 code
- Invisible bridge between DAQ MB and PCI

“DDU Not Yet Implemented”
- No Bunch Crossing Counter
- No High Level Error Checking (BX, Header Counts, etc.)
- No data processing
- After initial 16-20 Word burst, double-word rate is at most 16 MHz
DDU Hardware Status Summary
- Test Beam DDU version 1 (prototype) is under testing
  - Performing well with HP X’CVR @ up to 65 MHz
- Version 2 ready in 6 - 8 weeks
  - no new features
  - will work at full 75 MHz
- Full version (with all “features”) still on drawing board

DDU Device Driver Status
- Currently uses standard AMCC V ID/DID -- hope it is unique
- Currently supports one card
- Burst capable, although burst writes have timing problems (ok - they aren’t used for data gathering)
- Needs to be integrated into DAQ software

Contact Me -- I’d love to hear from you: nylander@mps.ohio-state.edu